UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/598,173	06/21/2000	Bernd Moller	2789-17	6943

7590 03/19/2004

Nixon & Vanderhye PC
8th Floor
1100 North Glebe Rd
Arlington, VA 22201-4714

EXAMINER	
PATEL, NITIN C	

ART UNIT	PAPER NUMBER
2116	17

DATE MAILED: 03/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/598,173	MOLLER ET AL.	
	Examiner	Art Unit	
	Nitin C. Patel	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8-22 and 24-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-22 and 24-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *16*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This is in responsive to RCE with pre-amendment filed on March 05, 2004.

2. Claims 7, and 23 have been cancelled.

3. Claims 1 – 6, 8 – 22, and 24 – 30 are presented for examination.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 1 – 6, 8 – 22, and 24 – 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gilberg et al. [hereinafter as Gilberg], US Patent 5,083,293 [cited in IDS in paper no. 16], and further in view of Chou et al. [hereinafter as Chou], US Patent 5,892,906.

7. As to claims 1, and 17, Chou teaches a computer system and method of preventing theft of computer device comprising: (a) a processor [14, CPU] for executing program routines [it is inherent property of CPU to execute program routines] executed by the processor, where processor is arranged to necessarily execute a security program stored in memory upon start-up

[col. 3, lines 52 – 67, col. 4, lines 1 – 19]. However, Chou teaches read only memory [ROM] from which data can be read only and is protected from being written into, but he does not disclose a memory arrangement with a protected part with mechanism provided such that after data is initially stored in protected part, any subsequent writing of data into the protected part is irreversibly blocked. In summary, Chou does not teach to protect a part of memory form subsequent writing into with irreversible blocking mechanism.

Gilberg teaches a data processing system and method to prevent alteration of data that is stored in secured area of integrated memory chip with a mechanism of applying an "erase" signal to the erase terminal [66] to erase the contents of erasable memory [52] once data is stored in secured memory [M, fig. 1- 2] thereby prevent alteration of the secured data stored in secured part of memory [col. 1, lines 31 – 52, col. 2, lines 38 – 67, col. 4, lines 39 – 43].

It would have been an obvious to one of an ordinary skill in art at the time of invention to combine teachings of Chou for providing a security through BIOS with security routine within the BIOS routine in ROM and Gilberg's teaching with a mechanism to prevent alteration of data stored [BIOS with security routine] in secured locations because both are related to problems with security of processing system and a mechanism with fuse element for irreversibly altered state in response to control signal will secure data from any attack short of an extremely precise X-ray beam or other complex means that may be used to remotely program the erasable memory [col. 2, lines 2 – 8, col. 4, lines 50 – 54].

8. As to claims 2, and 18, Chou discloses that processor stores permanent start addresses that are necessarily called upon start-up of the processor [it is inherent to BIOS routine program

to call upon the start address], and obvious to one of an ordinary skill in art to points to protected [secured] part of the memory.

9. Claims 3 – 5, and 19 – 21, are rejected under 35 U.S.C. 103(a) as being unpatentable over Gilberg et al. [hereinafter as Gilberg], US Patent 5,083,293 [cited in IDS in paper no. 16], as applied to claims 1, 17 above, and further in view of Chou et al. [hereinafter as Chou], US Patent 5,892,906.

10. As to claims 3 – 5, and 19 – 21, Chou teaches execution of security program routine within BIOS routine [executed upon processor start-up] for authentication with calculating a characteristic parameter [product formed from serial number read and computer's I.D.] for data being checked for changes, by comparing the characteristic parameter with value stored [contents of key ROM][col. 4, lines 1 – 19].

Gilberg teaches a data processing system and method to prevent alteration of data that is stored in secured area of integrated memory chip with a mechanism of applying an "erase" signal to the erase terminal [66] to erase the contents of erasable memory [52] once data is stored in secured memory [M, fig. 1- 2] thereby prevent alteration of the secured data stored in secured part of memory [col. 1, lines 31 – 52, col. 2, lines 38 – 67, col. 4, lines 39 – 43].

It would have been an obvious to one of an ordinary skill in art at the time of invention to combine teachings of Chou for providing a security through BIOS with security routine within the BIOS routine in ROM and Gilberg's teaching with a mechanism to prevent alteration of data stored [BIOS with security routine] in secured locations because both are related to problems with security of processing system and a mechanism with fuse element for irreversibly altered state in response to control signal will secure data from any attack short of an extremely precise

X-ray beam or other complex means that may be used to remotely program the erasable memory [col. 2, lines 2 – 8, col. 4, lines 50 – 54].

11. As to claims 6, and 22, Gilberg discloses plurality of memory devices [EPROM, EEPROM, ROM], one of which comprises the protected [secured] part [area][col. 3, lines 37 - 43].

12. As to claims 8, and 24, Gilberg discloses that writing data into protected [secured] part [area] via a write line [64, write pulse], and sending a signal [control signal] to the protected [secured] part [area] the write line is permanently interrupted [once state of fuse element is irreversibly changed in response to control signal, decoder 40 prevents writing any further data into predetermined location][col. 3, lines 22 – 26].

13. As to claims 9, and 25, Gilberg discloses that write line [write pulse] is a fusible link [60][fig. 2].

14. As to claims 10, and 26, Gilberg, discloses a decoder [40] to prevent the writing of any further data into predetermined memory location once state of fuse element [42] is irreversibly changed [col. 3, lines 23 – 26] which can be implemented with the use of state machine logic too.

15. As to claim 11, and 27, Gilberg discloses ROM, EEPROM and flash memory [col. 3, lines 37 - 43].

16. As to claims 12, and 28, it is inherent to the assembly process or component mounting on board to have memory chip having electrical contacts for being connected to the circuit board.

17. As to claims 13, and 29, it is inherent to provide electrical contacts to the ball grid array [BGA] components.

18. As to claim 30, Chou discloses a readable medium [ROM] by a processing device having a program [BIOS program] recorded [stored] thereon, where the program is to make the data processing device [CPU] to execute [it is inherent to CPU to execute the BIOS program stored].

19. As to claims 14 – 16, and 30, Chou teaches computer system with CPU for data processing which, is applied to different communication device [mobile telephone] with different communication protocol.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin C. Patel whose telephone number is 703-305-3994. The examiner can normally be reached on 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 703-305-9717. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nitin C. Patel
March 17, 2004

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100